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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,945	LIAW, JHON JHY	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *18,22,24-30,32-36,38-45,47 and 49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18, 22, 24-30, 32-36, 38-45, 47 and 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination, for which this application is eligible, under 37 CFR 1.114, including timely payment of the fee set forth in 37 CFR 1.17(e), was filed in this application (02/28/2008) after final rejection. The finality of the previous Office action has been withdrawn. Applicant's submission filed 01/08/2008 has been entered.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 18-22, 24-25, 27-30, 32-35, and 38-45, 47, 49 and 50 are rejected under 35 U.S.C. 103(a) as being obvious in view of Tamaru (US 2003/0030146) and Chen (US 6,784,096).

Re claim 18, Tamaru discloses a contact interconnect structure comprising (e.g., Fig 14, ¶72):

a semiconductor substrate (1: ¶73 ln 2) comprising CMOS devices (¶78 ln 11-12) including active contact regions (11, 12: ¶77);

a first contact layer overlying the active contact regions comprising a first plurality of metal filled contact openings (18 filled 17: ¶79 ln 7-8) extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer comprising a second plurality of metal filled contact openings (24 filled 22: ¶87 ln 2), each of said second plurality of metal filled contact openings extending through the second contact layer thickness to physically contact a major metal filling portion of a respective one or more of the first plurality of metal filled contact openings;

wherein the first plurality and the second plurality of metal filled contact openings form a physically continuous contact interconnect structure, said first and second metal filled contact openings having an aspect ratio of less than about 4.5 with respect to a respective contact layer, said contact interconnect structure connecting said active contact regions to overlying wiring circuitry comprising metallization layers (33; ¶95).

Tamaru differs from the claimed invention only in not expressly disclosing the value of the aspect ratio.

Chen discloses a contact interconnect structure having an aspect ratio less than about 4.5 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, the continuous contact interconnect structure of Tamaru have an aspect ratio less than about 4.5 with respect to a respective contact layer; at least to reduce device size.

Re claim 19, Tamaru as modified by Chen above discloses the bottom portion of said contact interconnect structure has a maximum width (inherent) and an aspect ratio of less than about 4.5

Tamaru as modified by Chen differs from the claimed invention only in not expressly disclosing the width of said interconnect structure.

Chen discloses a contact interconnect structure having a maximum width of less than about 70 nanometers (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, the bottom portion of said contact interconnect structure of Tamaru has a maximum width of less than about 70 nanometers; at least to reduce device size.

Re claim 20, Tamaru discloses an overlying metallization layer (33) in electrical communication with the second plurality of metal filled contact openings.

Re claim 21, Tamaru discloses the first (16) and second (20) contact layers are selected from the group consisting of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, fluorine doped silicon oxide, SiC, silicon nitride, and silicon oxynitride (¶79 ln 21-26, ¶80 ln 2).

Re claim 22, Tamaru discloses the first and second contact layers comprise lowermost portions (15 and 19) of silicon nitride (¶79 ln 1, ¶80 ln 1).

Re claim 24, Tamaru discloses the first plurality and the and second plurality of metal (18 and 24) filled contact openings comprise conductive materials selected from the group consisting of Cu, W, Al, AlCu, TiN, TiW, Ti, TaN, and Ta (¶79 ln 14-17; ¶87 ln 1-5 and ¶88 ln 6-11).

Re claim 25, Tamaru discloses (Fig 12) the active contact regions are source and drain regions (¶77 ln 6-8).

Re claim 27, Tamaru discloses the active contact regions comprise a conductive material of $CoSi_2$ (¶78).

Re claim 28, Tamaru discloses the first and second contact layers comprise an uppermost portion selected from a hardmask layer and a BARC layer (understood to encompass the materials disclosed by Tamaru, e.g., Fig 15: 19, 34, 21, 25, 35).

Re claim 29, Tamaru does not limit his metal filled opening to any particular shape, therefore the disclosure of Tamaru encompasses all well-known metal filled contact opening shapes, including circular.

Re claim 30, Tamaru discloses the first and second plurality of metal filled contact openings are selected from the group consisting of vias, contact holes, butt contact interconnects, local interconnects, and interconnect lines (¶79 ln 7, ¶86 ln 4).

Re claim 32, Tamaru discloses a contact interconnect structure comprising (e.g., Fig 14, ¶72):

at least first (16) and second (20) stacked contact layers comprising a respective first (18 filled 17) and second (24 filled 22) plurality of metal filled contact openings (¶79 ln 7-8, ¶87 ln 2) extending through the respective first and second contact layers to a contact region (11, 12) comprising an active transistor region (¶78 ln 11-12), said first and second plurality of metal filled contact openings forming physically contacted major metal filling portions comprising said stacked contact interconnect structure;

wherein, the first and second plurality of metal filled contact openings comprise a bottom portion (inherent) having a maximum width, said first and second metal filled contact openings having an aspect ratio with respect to a respective contact layer, said

contact interconnection structure connecting said active contact regions to overlying wiring circuitry comprising metallization layers (33; ¶95).

Tamaru differs from the claimed invention only in not expressly disclosing either the maximum width or the aspect ratio.

Chen discloses a contact interconnect structure and teaches an opening width of less than about 70 nm and an aspect ratio of less than about 3.3 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, said bottom portions of Tamaru have a maximum width of less than about 70 nanometers and an aspect ratio of less than about 3.3 with respect to a respective contact layer; at least to reduce device size.

Re claim 33, Tamaru differs from the claimed invention only in not expressly disclosing either the maximum width or the aspect ratio.

Chen discloses a contact interconnect structure and teaches an opening width of less than about 50 nm and an aspect ratio of less than about 4.5 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, said bottom portion of Tamaru has a maximum width of less than about 50 nanometers and an aspect ratio of less than about 4.5; at least to reduce device size.

Re claim 34, Tamaru discloses the first and second contact layers comprise an underlying-etch stop layer (e.g. Fig 15: 15 and 34).

Re claim 35, Tamaru discloses the active contact regions are source and drain regions (¶77 ln 6-8).

Re claim 38, Tamaru discloses a stacked contact interconnect structure for achieving a high aspect ratio (e.g., Fig 14, ¶72):

a semiconductor substrate (1: ¶73 ln 2) comprising CMOS devices (¶78 ln 11) including active contact regions (11, 12: ¶77);

a first contact layer overlying the active contact regions comprising a first metal filled contact opening (18 filled17: ¶79 ln 7-8) extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer comprising a second metal filled contact opening (24 filled 22: ¶87 ln 2), extending through the second contact layer thickness to physically contact a major metal filling portion of the first metal filled opening;

wherein, each of the first and second plurality of metal filled contact openings have about the same width to form a physically connected stacked contact interconnect structure, said first and second metal filled contact openings having an aspect ratio with respect to a respective contact layer, said contact interconnection structure connecting said active contact regions to overlying wiring circuitry comprising metallization layers (33; ¶95).

Tamaru differs from the claimed invention only in not expressly disclosing the value of the aspect ratio.

Chen discloses a contact interconnect structure having an aspect ratio less than about 4.5 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, the stacked contact interconnect structure of Tamaru have an aspect ratio less than about 4.5 with respect to a respective contact layer; at least to reduce device size.

Re claim 39, Tamaru discloses a bottom portion of said contact interconnect structure (inherent).

Tamaru differs from the claimed invention only in not expressly disclosing either the maximum width or the aspect ratio.

Chen discloses a contact interconnect structure and teaches an opening width of less than about 70 nm and an aspect ratio of less than about 4.5 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, said bottom portions of Tamaru have a maximum width of less than about 70 nanometers and an aspect ratio of less than about 4.5; at least to reduce device size.

Re claim 40, Tamaru discloses the first (16) and second (20) contact layers are selected from the group consisting of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, fluorine doped silicon oxide, SiC, silicon nitride, and silicon oxynitride (¶79 ln 21-26, ¶80 ln 2).

Re claim 41, Tamaru discloses the first and second contact layers each comprise a lowermost etch stop layer (15 and 19) of silicon nitride (¶79 ln 1, ¶80 ln 1).

Re claim 42, Tamaru discloses the first plurality and the second plurality of metal (18 and 24) filled contact openings comprise conductive materials selected from the

group consisting of Cu, W, Al, AlCu, TiN, TiW, Ti, TaN, and Ta (¶79 ln 14-17; ¶87 ln 1-5 and ¶88 ln 6-11).

Re claim 43, Tamaru discloses the active contact regions are source and drain regions (¶77 ln 6-8).

Re claim 44, Tamaru discloses the active contact regions comprise a conductive material of $CoSi_2$ (¶78).

Re claim 45, Tamaru discloses the first plurality and the second plurality of metal filled contact openings comprise the same metal filling (TiN, ¶79 ln 15, ¶88 ln 8).

Re claim 47, Tamaru discloses the first and second plurality of metal filled contact openings comprise same major metal filling material (TiN, ¶79 ln 15, ¶88 ln 8).

Re claim 49, Tamaru discloses the first and second plurality of metal filled contact openings comprise same major metal filling material (TiN, ¶79 ln 15, ¶88 ln 8).

Claims 26 and 36 are rejected under 35 USC 103(a) as being unpatentable over Tamaru and Chen as applied respectively to claims 25 and 35 above, and further in view of Ono (IEEE Transactions on Electron Devices, V.42, N.10, Oct. 1995, pg.1822).

Re claims 26 and 36, Tamaru as modified by Chen differs from the claimed invention only in not disclosing a gate length of less than about 45 nm.

Ono discloses a MOSFET (Fig 2a) with a gate structure having a gate length of less than about 45 nm (caption).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Ono, the gate electrode of Tamaru comprises a gate length of less than about 45 nm, at least to reduce device size.

Response to Arguments

Applicant's arguments filed 01/08/2008 have been fully considered but they are not found persuasive.

The arguments that Tamaru does not teach the claimed contact interconnect structure and contact openings are not persuasive. Neither the claim language nor the record precludes reading the claims onto the structure of Tamaru.

The arguments concerning Chen are not convincing. Expectation of success is evident in their analogous concern with wiring schemes, and Chen teaches increased density (col 1 ln 50-55).

The argument that Ono does not teach an “interconnect structure" (pg 18 ¶4) does not seem significant since Ono is not relied upon for this feature, found in Tamaru.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571)272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval system. PAIR info: http://pair-direct.uspto.gov. For questions on access to Private PAIR, contact 866-217-9197 (toll-free). For assistance from a USPTO Customer Service Rep or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew O. Arena/
Examiner, Art Unit 2811
31 March 2008

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811